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DESIGN TECHNIQUES FOR MINIATURIZED
SPACECRAFT HIGH VOLTAGE POWER SUPPLIES

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Abstract

High voltage power supplies used in experiments on board unmanned scientific satellites must meet stringent requirements in the areas of size, weight, and efficiency. Careful selection of a design approach must be made in order to achieve these requirements and at the same time maintain high reliability. This selection is especially critical with today's output levels often being an order of magnitude higher than those called for in the past. This paper describes three high voltage power supplies that illustrate the different design requirements encountered in spaceflight applications and the appropriate circuit solutions.

1. INTRODUCTION

The areas addressed in this paper are derived from the results of detailed analysis coupled with breadboard experimentation in the development of high voltage power supplies. These areas in the past have been the sources of some design difficulties and/or a lack of understanding. With this understanding and the application of the results presented here, typical problems and pitfalls often experienced in these areas will be, hopefully, avoided.

Over the past 15 years or so, the Payload Interfaces and Instrument Power Section at the Goddard Space Flight Center has designed and provided a diverse array of high voltage power supplies for spacecraft experimenters. These have been designed to meet a wide variety of specifications supplied by the user to meet the particular requirements of the experiment. Three typical specifications recently designed to by this group appear (in abbreviated form) in Section 2. This is typical of the differences in requirements from one unit to the next. While it may be possible to copy

all or most of a past design for a specific job, it is obvious no one supply could practically serve all the needs shown by the three specifications. Because of this, and the ever-increasing demands of experimenters for more sophisticated and unique performance, more often than not each new requirement needs a new design effort.

However, all is not quite as gloomy as the above may imply. While it is true that a high voltage power supply may be a new design when taken as a whole, it will be made up of building blocks, the design and use of which can be based on practical experience from previous work. This is true particularly of those building blocks germane to the high voltage area. This paper deals with these areas, i.e., dealing with problems arising from the reactive loading of tuned circuits, isolated voltage regulation techniques, and performance prediction from the analysis of various forms of the basic multiplier stack. In regard to this last point, while it is true that certain aspects of multiplier design are well documented,

the authors have found that a complete overview of all operating characteristics of various stack configurations either does not exist or is very hard to find.

The questions to be answered here, therefore, are:

- (1) What characteristics should be looked for in selecting an AC generator as the initial stage of high voltage designs?
- (2) What considerations must be taken into account when dealing with reactively loaded tuned circuits?
- (3) What are some proven techniques for DC isolated voltage regulation?
- (4) What considerations are involved in multiplier stack configuration, and how does one analyze its operation to predict its performance?

2. The high voltage power supply primary specifications are shown in Table 1.

Any item not mentioned in Table 1 was either not specified, or not pertinent to this discussion. Figure 1 is a block diagram representation of a typical high voltage power supply. These can be considered as the basic building blocks of a typical high voltage power supply alluded to earlier.

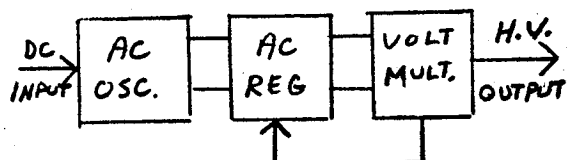


FIGURE 1

As will be shown, in some designs the last two blocks may be combined. Figures 17, 18, and 19 show, in simplified schematic form, the three high voltage power supplies. The following sections discuss the building blocks individually and their interactions.

3. VOLTAGE MULTIPLIERS

Cockcroft Walton Multiplier design characteristics have been described in numerous articles. (1,2) Normally derived are the losses and ripple generated to support a dc load according to the following equations:

TABLE 1

Power Supply	#1	#2	#3
Input Voltage	-24.5V \pm 2%	+28V \pm 10%	+19V \pm 2%
Output Voltage	\pm .5V to \pm 2500V programmably controlled by 6 bit serial cmd. to up to 60 Log. related levels per second	-35KV	0 to -24KV in 1024 steps commandable by 2 10 bit serial or parallel cmd.
Settling Time	\leq 2msec between sequential steps	-	-
Output Load	100namp @ 2500V.	0	40 μ amp @ -24,000V.
Regulation	+V and -V to differ \leq 2 %, (+V + -V) / 2 \leq % of commanded level	\pm 5%	\pm 0.05%
Output Ripple	\leq 5mv p-p	\leq 200V o-p	\leq 1V p-p
Frequency	20KHZ or multiple thereof	20KHZ or multiple thereof	—
Current Limit	—	$I_{in} \leq$ 25ma	—

$$V_{OUT DC} = 2NV_s \quad (1)$$

$$V_{RIPPLE} = (I/2fcN)(N+1) \quad (2)$$

$$V_{LOSS} = (I/fc)(2/3N^3 + 1/2N^2 - 1/6N) \quad (3)$$

Where - I = Load current
 f = Operating frequency
 c = Multiplier capacitance of each stage
 N = Number of stages
 V_s = AC Input Voltage 0 to Peak
 A stage is defined to mean what is commonly known as a doubler.

With a given load current, input voltage and output level, the two variables open to the designer to meet voltage loss and ripple goals are the operating frequency and capacitor size. As shown in the specifications Table 1, the operating frequency is sometimes restricted so the primary method to improve voltage ripple and loss is to vary the multiplier capacitance.

An alternative method to improve operating characteristics is to consider a modified multiplier circuit. Figure 2A shows the standard Cockcroft/Walton multiplier, and Figure 2B shows another version called the parallel charge multiplier.

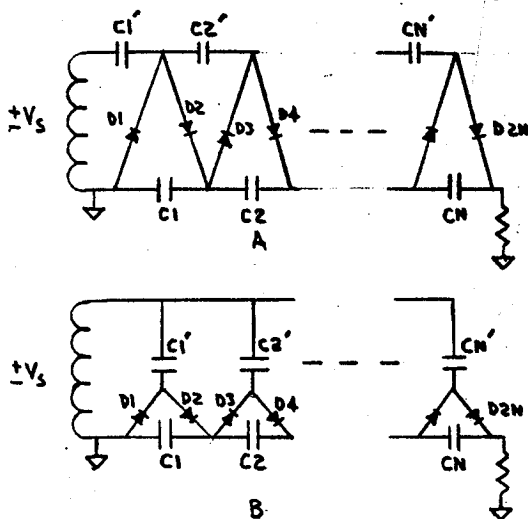


FIGURE 2

The parallel charge multiplier offers a reduction in the voltage loss as function of the number of stages over the Cockcroft/Walton multiplier without an increase in the number of parts.

To formulate ripple and loss equations for this multiplier similar to equations (3) and (2), a look at the charge transfer in the capacitors to support a load current is necessary.

If the amount of charge flowing from capacitor C_N to support the load current for one cycle is Δq . This charge, Δq , will be replaced from C_N' when V_s reaches a positive peak. Similar to a Cockcroft/Walton multiplier, the charge flow from C_{N-1} is $2\Delta q$. One Δq supports the load and the other Δq charges C_N' when V_s reaches its negative peak. However, the charge from C_{N-1}' to recharge C_{N-1} is one Δq . In the Cockcroft/Walton multiplier, the charge flow in C_{N-1}' is $2\Delta q$. One Δq flows into C_N' and another into C_{N-1} . The results of determining the charge flow per cycle for the rest of the multiplier is shown in Figure 3A and Figure 3B.

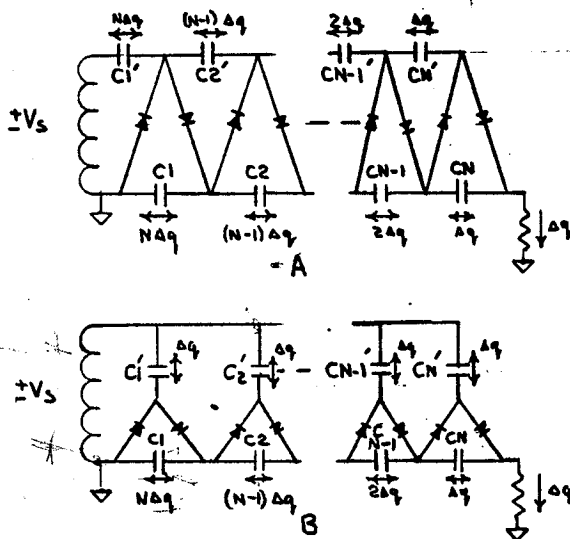


FIGURE 3

Although the charge transfer increases by one Δq in each of the $C_N, C_{N-1}, C_{N-2}, \dots, C_1$ stages as you progress up the stack, the charge transfer stays constant at one Δq in the upper capacitors $C_N', C_{N-1}', C_{N-2}', \dots, C_1'$.

As compared with the Cockcroft/Walton version where the charge transfer increases by one Δq in both the upper and lower capacitors, the voltage loss is

reduced (particularly for the stages nearest the input) when charge is passed from the upper to lower capacitors.

The loading drop for the parallel charge multiplier with all capacitors having equal value is calculated as follows:

C_1 is charged when V_s is at its positive peak to $2V_s - \Delta q/c$ because of the voltage given up by C'_1 equals $\Delta q/c$. C'_2 is then charged when V_s is at its negative peak to $2V_s - \Delta q/c - N\Delta q/c$ because of the charge reduction in C_1 is $N\Delta q/c$. Progressing down the multiplier in a similar fashion yields the following results:

$$V_{L1} = \Delta q/c = I/fc$$

$$V_{L2} = I/fc (1+N)$$

$$V_{L3} = I/fc (2N)$$

...

$$V_{LN} = I/fc (N + (N-1) + (N-2) + \dots + 1)$$

where V_{LN} is the dc loss in the nth stage.

The total loss is:

$$\begin{aligned} V_{L \text{ TOTAL}} &= V_{L1} + V_{L2} + \dots + V_{LN} \\ &= I/fc \sum_{n=1}^N (n^2 - n + 1) \quad (4) \\ &= I/fc (N^3 + 2/3N) \quad (5) \end{aligned}$$

The ripple voltage would still be:

$$V_R = I/2fc N(N+1) \quad (6)$$

Use of the parallel charge multiplier involves a tradeoff with component voltage ratings. The voltage across the capacitors $C'_1, C'_2, C'_3, \dots, C'_N$ increase as follows:

$$V_{Cn}' = (2n-1)V_s \quad (7)$$

Use of the parallel charge multiplier with high stage count could become prohibitive because of the required high voltage rating for the higher stage C' capacitors. The voltage across the C_1, C_2, \dots, C_N capacitors is $2V_s$. In a Cockcroft Walton multi-

plier the maximum voltage across any capacitor is $2V_s$.

However, the problem of increasing voltage stress can be overcome. With a parallel charge multiplier, since the upper capacitors only pass one Δq , a smaller value capacitor could be used with a higher voltage rating for the latter stage without greatly sacrificing performance and increasing part size. For this arrangement, Fig. 4, the voltage loss is calculated to be:

$$V_{\text{loss}} = I/fc (N^3/3 - N/3 + N/a) \quad (8)$$

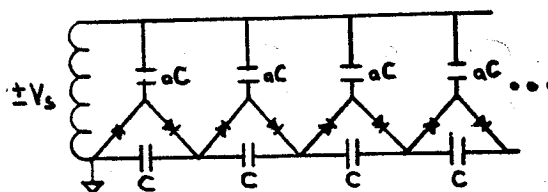


FIGURE 4

The increase of loss over the standard parallel charge multiplier is eq.(8)- eq.(5) or

$$V_{\text{diff}} = NI/fc (1/a - 1) \quad (9)$$

For an example, suppose $N=10$, $1/a=10$, and $I/fc=1$. The losses for the three multipliers with an output voltage of 12.5KV would be:

MULTIPLIER	LOSS (volts)
Cockcroft Walton	715
Parallel Charge	340
Par. Charge With $C'_n = C/a$	430

Other multiplier configurations are available to the designer. Hybrid multipliers which cascade together parallel charge and Cockcroft Walton stages can offer intermediate performance while limiting component rating increases. Examples are illustrated in figure 5.

Taking a closer look at Fig. 5B, one can see that the multiplier consists of two three stage Cockcroft

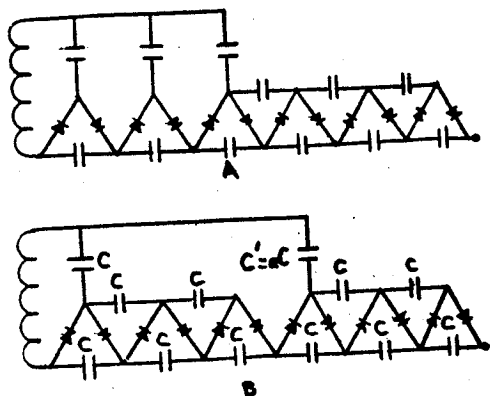


FIGURE 5 *series/parallel*

Walton multipliers connected in series. We'd like to compare the characteristics of this type network with two $N/2$ series stages to our previous stacks.

Calculating the voltage loss yields:

$$V_{\text{loss}} = I/fc [20/6(N/2)^3 + (N/2)^2/a - (N/2)/3] \quad (10)$$

Each capacitor sees a maximum voltage of $2V_s$ with the exception of C' , which sees a voltage of $(N+1)V_s$. This network provides improved performance over the standard Cockcroft/Walton multiplier and requires only one component with an elevated voltage rating above $2V_s$.

Figure 6 compares the four multipliers discussed as a function of the number of stages N .

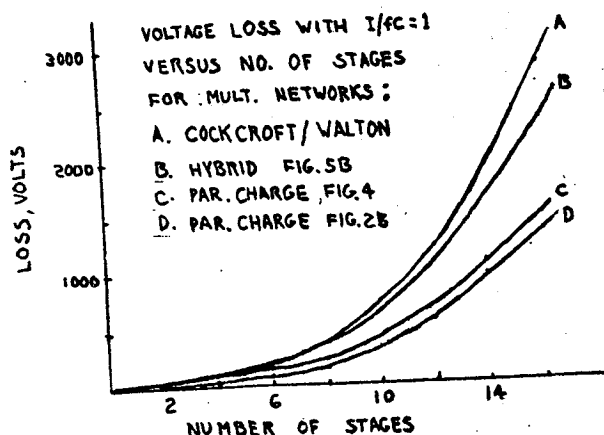


FIGURE 6

A second type of ripple voltage and voltage loss is generated in a multiplier stack from the circulating currents in the series and shunt (rectifier) capacitors. A cascaded multiplier actually forms a capacitor ladder network which attenuates the sine wave amplitude in each successive stage. This ripple is sinusoidal and exists with an amplitude independent of the load and operating frequency. This phenomenon was first described by Everhart and Lorrain³ and the following equations for voltage loss and ripple were developed:

$$V_{\text{out}} = V_s \tanh(2N/b) \quad (16)$$

$$V_{\text{ripple}} = V_s (1 - \text{sech}(2N/b)) \quad (17)$$

$$\text{where } C_{\text{DIODE}} = C_{\text{MULT.}}/b^2$$

A look at how this voltage ripple and loss are developed would be useful. Referring to figure 7, the AC voltage across D_1 in fig. 2A is attenuated to a level below $2V_s$ because of the divider action between C'_1 and the rest of the stack. If the ratio of the multiplier capacitance to the rectifier capacitance were infinite the sine wave voltage swing on D_1 and all other diodes would be $2V_s$.

When the input sine wave is at the negative extreme the voltage across D_1 reaches zero volts for multiplier action to exist. Since the voltage swing is less than $2V_s$, the peak voltage across D_1 is less than $2V_s$ by an amount Δ . At this time the voltage

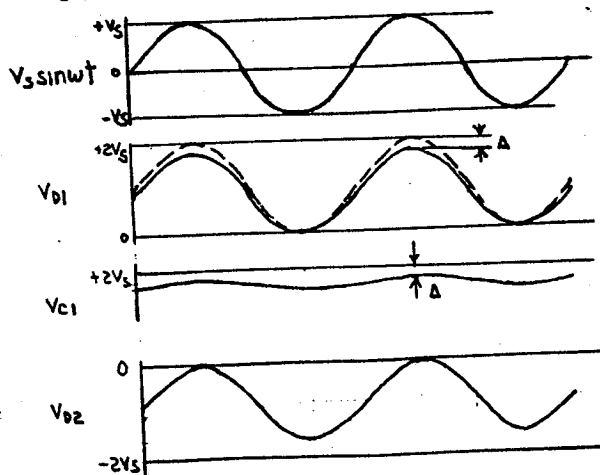


FIGURE 7

across D_2 is zero volts and the voltage impressed on C_1 is reduced by the same amount. As the input sine wave approaches its negative extreme the voltage across C_1 reaches a minimum again due to divider action. This produces a further voltage drop when D_3 conducts. The AC current flow in C_1 and the rest of the lower capacitors (C_2, C_3, \dots, C_N) produces the ripple voltage. The sinusoidal current that flows into the stack is essentially the current required to charge each of the diodes' parasitic capacitance and can be approximated by:

$$I_{\text{stack}} = (V_s)(j\omega 2NC_D)$$

or $C_{\text{stack}} = 2NC_D$ (11)

where C_D is the capacitance of each diode

The AC current in the multiplier capacitors is reduced for each succeeding stage since the number of diodes in the remainder of the stack reduces; or stated another way, the stages nearest the input contribute the majority of the total ripple voltage.

Worst case ripple can be estimated for multipliers with $b \gg 1$ by simply summing the voltage drop in each C_N due to current flow to charge the total diode capacitance in the remainder of the stack.

Approximately, the current flow into each diode is:

$$I = \omega V_D C_D$$

Through C_1 flows the current of $(2N-1)$ diodes resulting in a voltage drop (assuming V_D for all diodes equals V_s) equal to:

$$V_{R1} = (2N-1)\omega C_D V_s / \omega b^2 C_D = (2N-1)V_s/b^2$$

$$\text{and } V_{R2} = (2N-3V_3)/b^2$$

⋮

$$V_{RN} = V_s/b^2$$

The resultant total drop is $V_s N^2/b^2$ (12)

The same analysis for voltage loss due to shunt capacitance can be performed for the parallel charge multiplier. The results yield the following equation for output voltage:

$$V_{\text{OUT}} = V_s \sqrt{2} b \tanh(\sqrt{2} N/b) \quad (13)$$

Figure 8 compares the losses for a Cockcroft/Walton to a parallel charge multiplier.

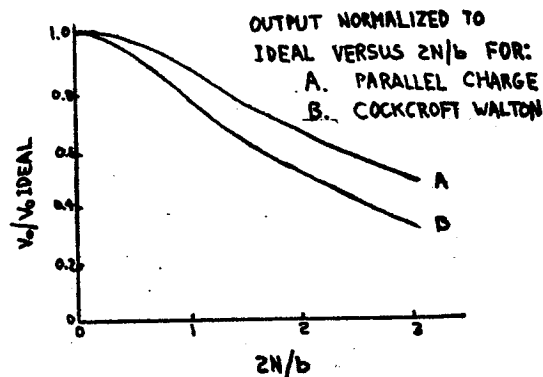


FIGURE 8

Now that a background is established in multiplier theory, we can proceed with the examination of the stacks for the three supplies.

The -35KV power supply multiplier has an input voltage of approximately 1600 volts 0 to peak and requires an output of -35,000 volts with less than 200 volts ripple 0 to peak.

Since the power supply operates under no load, a Cockcroft/Walton multiplier using $C_N = C_N' = 1,000$ pf and $C_D \sim 1.5$ pf can be used with no component rating exceeding $2 V_s$. The output drop and ripple can be computed using equations 16 and 17.

A twelve stage network would give an ideal output of $12 \times 2 \times 1600 = 38,400$ volts.

The DC output with losses would be:

$$V_{\text{OUT}} = 3200 + 1600 \sqrt{2000} \tanh(22/\sqrt{2000}) = 35,875 \text{KV}$$

$$V_{\text{RIPPLE}} = 1600 [1 - \text{sech}(2N/b)] = 187 \text{ volts o-p}$$

In this case, the Cockcroft/Walton multiplier would provide adequate results without requiring capacitor voltage ratings above 3200 volts.

The Stepping Power Supply requires a three stage multiplier to step up the transformer output level to approximately 3KV with a 500V 0 to peak input sine wave. Since the input to the multiplier is

stepped from one DC level to the next, and the settling time between steps is to be minimized, a stack offering minimum dynamic impedance is desirable.

A parallel charge multiplier would offer the best results. The equivalent impedance would be represented by $(N^3/3 + 2N/3)/f_c$ which was derived in equation 5. The output could then be written as:

$$V_{OUT} = 2NV_3 - I/f_c (N^3/3 + 2N/3) \quad (14)$$

Also apparent is the need to operate at the highest practical frequency. Because of space limitations, the capacitor size per stage is limited to 220 pf.

The equivalent impedance with the frequency at 60KHZ equals:

$$(N^3/3 + 2N/3)/f_c = (11)/60 \times 10^3 \times 220 \times 10^{-12} = 833K$$

Since the maximum amplitude of V_s is approximately 500 volts, the maximum required component rating is $500 \times 5 = 2500$ volts.

Calculating the ripple voltage due to the shunt capacitors with a 2500 volt output yields:

$$V_R = E (1 - \text{sech } 2N/b)$$

$$b^2 \sim 220/1.5 = 147$$

$$V_R = 500 (1 - \text{sech } 6/12.1) = 55 \text{ volts p-p}$$

The -24,000 volt power supply requires a cascade network of 10 stages and has to deliver approximately 1 watt. A standard Cockcroft/Walton circuit would contribute excessive drop with this stage count. The parallel charge multiplier would provide the necessary reduction in losses; however, five capacitors would have to support a voltage in the 12 to 24KV range. This arrangement would cause a size and weight problem. Figure 5B was chosen because only one capacitor would need to support a voltage of 13KV and the rest would support approximately 2.4KV.

The ripple^{is} calculated for the network as follows: First, the ripple voltage due to the loading effect with $C=4400\text{pf}$, $f=35 \times 10^3$, $I=40\mu\text{A}$.

$$V_R = I/f_c N(N+1) = 14 \text{ volts p-p}$$

The ripple due to the shunt capacitor is with

$$b^2 = 4400:$$

$$V_R = E (1 - \text{sech } 2N/b) = 1300 (1 - \text{sech } 20/66) = 57 \text{ volts p-p.}$$

The voltage output calculates to:

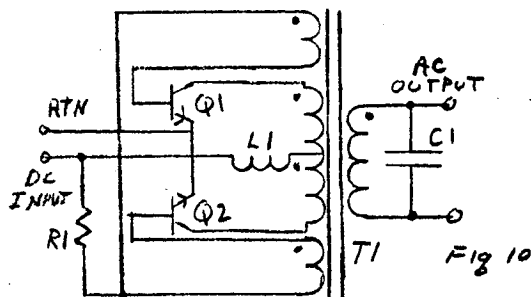
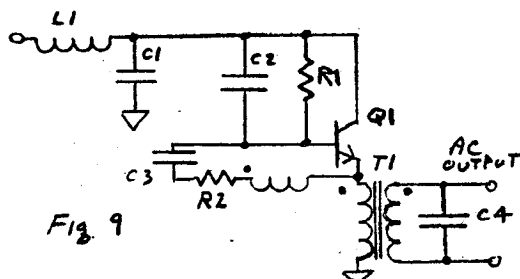
$$V_{OUT} = V_s b \tanh (2N/b) = 25,236 \text{ volts}$$

The loss calculated from equation 10 is 194 volts. so the total DC loss is $194 + 764 = 958$ volts.

4. OSCILLATORS

The AC generator is the basic building block from which the high voltage is ultimately developed. Resonant sine wave oscillators are generally preferred for this purpose. Driven sine wave generators, as well as driven and self-oscillating square wave generators have been used in the past for this purpose. These, however, generally give poor performance as they tend to be inefficient and, in the case of the square wave generators, very noisy.

Quite often in the past, very good use has been made of a single ended resonant sine wave oscillator of the Hartley configuration. This is shown in Figure 9. Its attraction lies chiefly in its efficiency, simplicity and consequent reliability. Its efficiency stems from Class C operation whereby Q1 conducts only briefly during that part of the cycle when its collector-emitter voltage is near zero volts. This type of oscillator does sometimes show temperamental operation in that it can display non-symmetrical waveforms and/or parasitic oscillations under certain conditions. Also, it tends to be somewhat sensitive to loading when transistor gain becomes quite significant and sometimes Q1 must be a compound connected pair of some sort.



FIGURES 9-10

The push-pull circuit shown in Figure 10 tends to overcome these problems. It is a self-resonant sine wave oscillator and with reasonable design displays very stable operation under all conditions. This is primarily due to the positive feed back Class B operation of Q1 and Q2. This circuit has been well documented.^(4,5) Input current to the primary is a fairly steady DC (depending on the size of L1). Very good efficiency is obtained since Q1 and Q2 are full on (saturated) during their conducting half of the cycle. The AC voltage is absorbed by the input choke L1. This means that energy is being pumped into the transformer at all times except the instant when the winding voltage is zero. At any instant, the power is being directly transformed to some load which may be across the secondary and/or stored in the circuits reactive elements. The input power to T1 is:

$$P_{in} = I_{in} \times E_{in}$$

or

$$P_{in} = I_{in} \times 2E_p/\pi \quad (15)$$

Where E_p is equal to one half of the peak collector voltage (or equal to the peak voltage across the "on" side of the transformer primary).

The resonant frequency is determined by the total capacitance reflected to any winding, and the inductance of that winding. In lightly loaded circuits, the capacitance could be only the winding capacitance plus stray capacitances. This can sometimes make the operating frequency hard to predict. When substantial loads are required (around one watt or more), then discrete capacitors should be added to the secondary and/or primary such that the RMS resonant current is about 10 times the DC input current (considering turns ratios). It has generally been found beneficial to have capacitance across both the primary and secondary under loaded conditions as it tends to reduce sine wave distorting, which in turn reduces the chances of parasitic oscillations appearing on the peak of the sine wave. A side benefit of this circuit is that no input filter capacitor is required. All three high voltage power supplies use this sine wave oscillator with good success.

5.

REGULATORS

High voltage regulation generally takes one of the two basic forms, series or parallel, and on occasion both may be used. Series regulation is often of the so called "front end" type whereby a series regulator is put at the input to the power supply and controlled by feedback from either the output itself, or some point before that. This technique has two disadvantages.

- (1) Inherent lack of DC isolation between input and output.
- (2) Inclusion of more of the complex AC circuitry in the feedback loop.

The first problem can be overcome with the use of such devices as opto-isolators. However, a more satisfactory solution to overcome both the above is to regulate somewhere beyond the sinusoidal oscillator. A technique which has been used extensively by this group is one in which a series regulator is placed between two transformers by means of a full wave diode bridge. This is shown in Figure 11A.

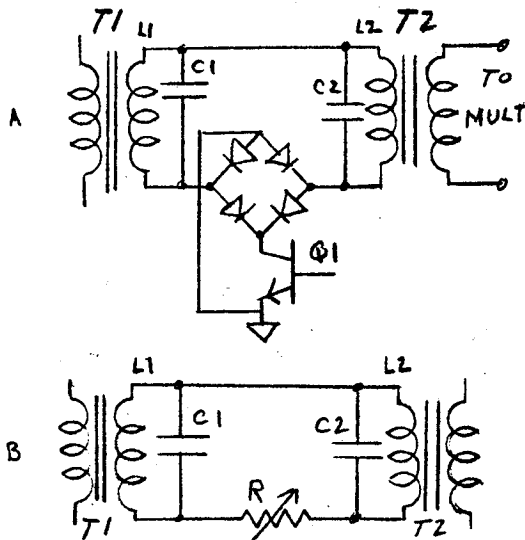


FIGURE 11

While this technique can introduce some problem, a good understanding of the pertinent circuit characteristics and proper design can give excellent results. An equivalent circuit is shown in Figure 11B.

This circuit has the advantage of much design flexibility. The turns ratios of T1 and T2 can be tailored over a wide range. Typically, T1 will give a peak AC output of about 150 volts. This is the maximum collector voltage which Q1 would normally be expected to see (see below). However, T1's output could be designed higher or lower depending on the available transistor voltage ratings. One point to bear in mind is that if Q1 is commanded off to reduce the output voltage to zero, its collector voltage will approach the peak to peak output from T1. This is because the diode junction capacitances in the full wave bridge tend to peak rectify and hold their reverse voltage since there is no where to discharge.

It is important to realize that if the resistor R in Figure 11B were equal to zero (regulating transistor full on), then T2 would combine in parallel with T1 to form an equivalent tuned circuit which would oscillate at a frequency determined by the combined effect of L1, L2, C1 and C2. However, the presence of resistor $R > 0$ tends to isolate somewhat the two transformers to a degree dependent upon the value of R. Therefore, the parallel resonant circuit of T2, in series with resistor R, form the load for the output of T1. In practice, T1 would be designed to operate at the desired frequency. T2 would be then designed to self-resonant at this same frequency. This will keep the reactive component of AC current to a minimum, and in phase with the output voltage from T1 and the voltage across T2 (i.e., T2 impedance is resistive and at a maximum). This will result in the most efficient transfer of energy from the AC oscillator to the multiplier stack.

Also, the frequency of oscillation will stay essentially fixed independent of the value of R (regulated level). It is somewhat difficult to predict exactly what T2 will have for a self-resonant frequency. Usually, C2 is not a discrete capacitor and is made up of total winding capacitance, and whatever capacitance is introduced by the multiplier stack (eq. 11). Potting will usually tend to increase the capacitance somewhat.

It is advisable to individually pot T1 and T2 and try them prior to final total encapsulation. If an impedance meter of some sort is available, it is handy for checking the post-potted resonant frequency of T2. A rule of thumb could be to reduce this by about 20% to allow for the effects of a typical multiplier stack and further potting. One technique sometimes useful is to purposely design T2 to a higher frequency than T1, say 1.5 to 2 times, and then reduce it by the addition of discrete capacitance for C2, adjusting until maximum efficiency is obtained. For those inexperienced in this area, some trial and error is usually required. Power supply No. 1 and No. 3 use this technique.

Another class of isolated series regulators is available that does not require two transformers. The regulator is included as part of the multiplier. Figure 12 illustrates one type used with a doubler multiplier. In some applications, this arrangement can save volume and weight.

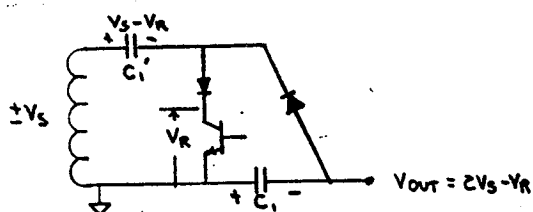


FIGURE 12

The voltage across C_1 is limited to $V_S - V_R$. The output is then controlled to $2V_S - V_R$. The efficiency of this circuit is approximately the same as the two transformer regulators, and is approximately $= 1 - V_R/2V_S$.

The voltage across Q1 is now higher, typically 1,000 volts. Transistors with lower V_{CB} breakdown ratings can be used by using a series arrangement as illustrated in Figure 13.

A second version can be used to regulate a multiplier stack with a high stage count. It is illustrated in Figure 14.

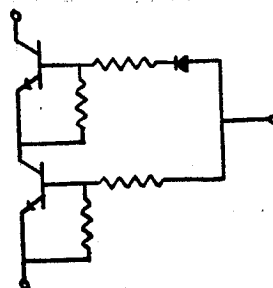


FIGURE 13

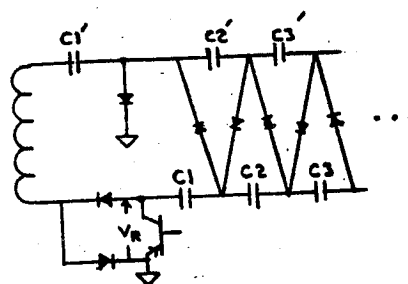


FIGURE 14

Again C_1 is limited to $V_S - V_R$. The output of the Nth stage is controlled to $N(2V_S - V_R)$. The same requirement of a high voltage pass transistor or equivalent is necessary.

One advantage of regulating in the multiplier is that the phase margin of the feedback loop is increased because the control is performed with fewer phase shifts.

When the AC input to a multiplier is stepped from one level to lower level, the fall time of the output is determined by the RC time constant of the multiplier and the load. For lightly loaded outputs, this time constant can be tens or hundreds of milliseconds.

In the stepping power supply (No.1), the fall time of an output step change is to be less than one millisecond. In order to meet this response time a shunt regulator, in addition to the series regulator, is used as illustrated.

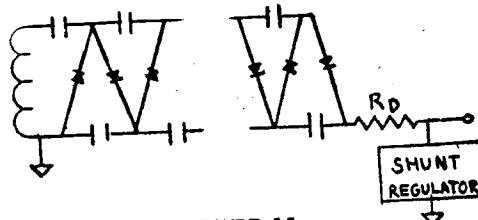
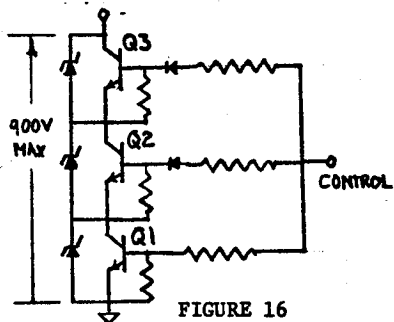


FIGURE 15

The multiplier output DC level is stepped to reduce dissipation in RD. Its level is kept approximately 300 volts above the shunt regulator output by means of the series regulator. The series regulator provides the coarse preregulated input to the shunt regulator, which fulfills the rest of the response requirement.

The shunt regulator's response to a commanded level change is extremely fast and assuming a typical output line capacitance of 100 pf, the settling time from one step to the next is approximately 1 msec.

Figure 16 shows a typical high voltage shunt regulator. The transistors are connected in a "Totem Pole" configuration.



The zener diodes across each transistor limit the maximum collector to emitter voltage. With no bias on the control input Q1-Q3 are off, and the voltage out is determined by the zener diodes (typically, 300 volts each). As the bias is increased, Q1 conducts and saturates. Then Q2 enters the active region and also saturates when enough bias is applied. Similarly, Q3 starts to conduct and with enough bias Q3 saturates. So the shunt regulator can give us control of the output from the total zener diode drop (in this example, approximately 900 volts) to approximately zero volts. The "Totem Pole" configuration can be extended with more stages for applications with high output voltages.

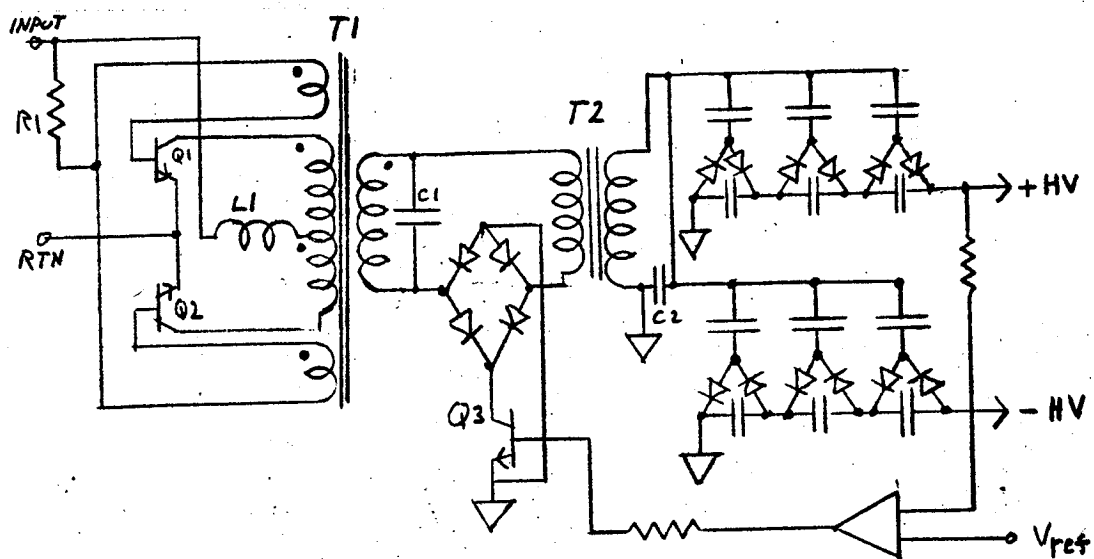
6.

CONCLUSIONS

The quest to improve the efficiency and reliability of high voltage power supplies is never ending. While the electronics involved in high voltage generation generally follows standard design rules and techniques, the physics of high voltage introduce problems which set this branch of electronics design uniquely apart from other areas. Engineers involved in high voltage work must not only have an excellent grasp of electronics theory and circuitry useful in this area, but must also be well versed in (1) materials and (2) the fabrication techniques required in this discipline. While much information on various aspects of high voltage design can be found, it is of a decentralized and disorganized nature. This paper was written with the hope it would be of some assistance in the electronics area.

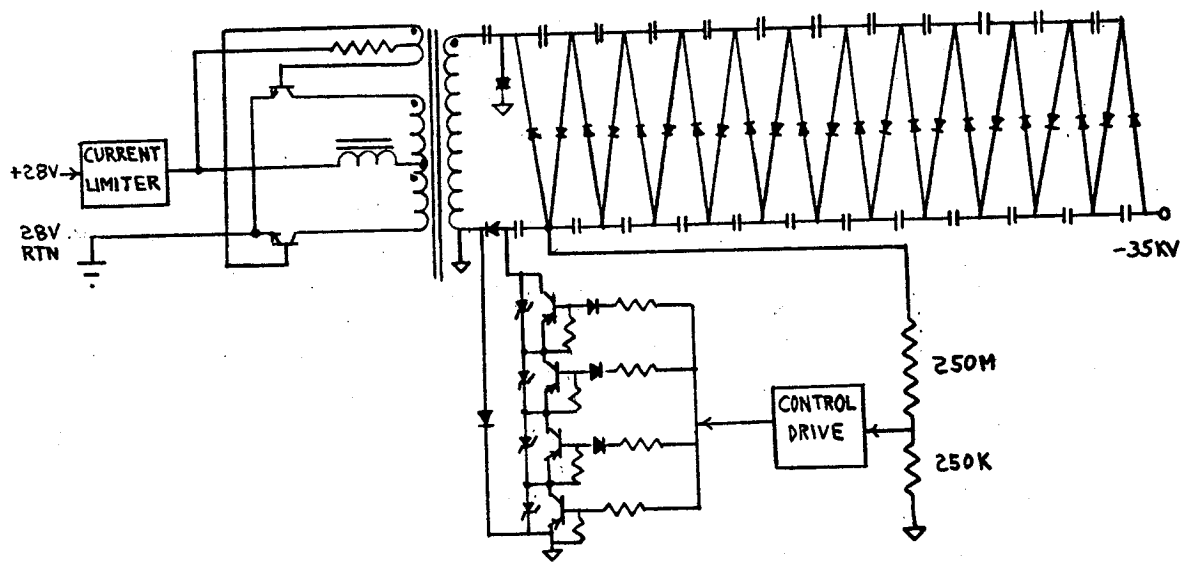
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P.S. #1 STEPPING POWER SUPPLY

FIGURE 17



P.S. #2 -35KV POWER SUPPLY

FIGURE 18

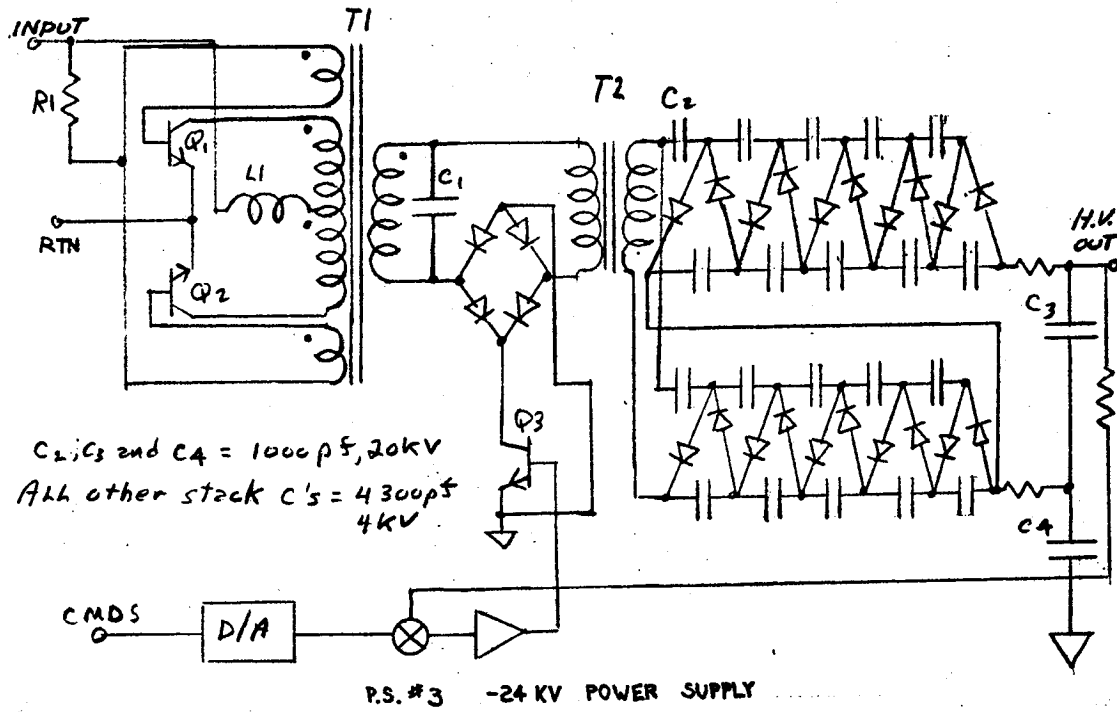


FIGURE 19

(13)

